REMARKS

This amendment is filed in response to the Office Action filed August 18, 2002. All objections and rejections are respectfully traversed.

Claims 1-35 are in the case.

Claim 35 was added to better claim the invention.

At paragraph 1 of the Office Action the examiner noted that the reply filed on May 21, 2002, did not point out the patentable novelty of the newly presented claims, claims 20-34, and required such a presentation pursuant to MPEP 714.04.

The present invention, as set forth in representative claim 20, comprises in part:

> 20. A processor comprising:
> an execution unit having an input and an output;
> an input register connected to said input and said output of said execution unit; and
> ***a register decode value that specifies bypassing data from said output of said execution unit to said input register during a write back cycle transferring said data to a register file.***

Asato teaches a data processing device having a bypass function that analyzes the dependency of instructions in a limited range of a processing device with a pipeline bypass function, by making comparisons between destination addresses and source addresses of different instructions. In several embodiments, software is used to determine values of additional fields in the opcode (such as b1, b2, p1 and p2) which determine if bypass of values from other registers along the pipeline would occur. In at least one em-

bodiment, which does not utilize these additional fields in the opcode, dedicated logic is used to determine if the source and destination fields between overlap over a range of consecutive instructions. In all embodiments, the values of these fields or the value produced by the dedicated logic control a subsystem of dedicated logic that determine the input to multiplexers controlling various stages of the pipeline and bypassing between said stages.

Applicants respectfully urge that Asato does not show applicants' claimed novel "***a register decode value that specifies bypassing data from said output of said execution unit to said input register during a write back cycle transferring said data to a register file***". Applicant's processor uses bypass determined by using different register decode values for different source operands. Applicant uses ***a register decode value that specifies bypassing data from said output of said execution unit to said input register during a write back cycle transferring said data to a register file.***

Applicant respectfully urges that Asato, by making comparisons between destination address and source address of different instructions, does not disclose applicants claimed novel register decode value used to specify bypassing data from an output of the execution unit to an input register during a write back cycle.

Further, applicants claimed novel invention, as set forth in representative claim 26, comprises in part:

> 26. A processor comprising:
> a first execution unit having at least one first input and a first output;
> at least one second execution unit having at least one second input and a second output;

a first input register connected to said at least one first input;

a second input register;

a multiplexer having a first input from said first input register, a second input from said second input register, and an output to said at least one second execution unit; and

a register decode value that specifies bypassing data from said first input register to said at least one second execution unit via said multiplexer.

Again, applicant respectfully urges that the Asato patent does not disclose a "***register decode value that specifies bypassing data from said first input register to said at least one second execution unit via said multiplexer***". Accordingly, applicant's respectfully urges that the claimed invention is patentable over the Asato patent.

Applicant respectfully urges that claims 34 and 35 are patentable in view of the allowability of method claim 9, see MPEP section 2106.

All independent claims are believed to be in condition for allowance.

All dependent claims are believed to be dependent from allowable independent claims, and therefore in condition for allowance.

Favorable action is respectfully solicited.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

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